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# Designing the Widlar current mirror

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**Abstract** The Widlar current mirror, a widely used integrated circuit configuration, normally receives only a superficial treatment in electronics texts. This didactic study consists of a detailed analysis followed by a step-by-step design procedure that takes into account resistor and transistor parameter tolerances, a topic rarely covered in undergraduate/graduate courses.

**Keywords** current mirrors; electronics teaching

How would you set about designing a direct current generator to produce a current in the microampere range without using resistors having high ohmic values?

This was a problem faced by analogue IC designers who had to take into account the fact that resistors greater than about 50k $\Omega$  took up chip-surface areas disproportionately large compared with that of a bipolar junction transistor (BJT). An elegant solution was devised by R. J. Widlar,<sup>1</sup> a pioneer of IC operational amplifier design, with a configuration subsequently named after him.

Although designers of systems incorporating discrete components do not suffer from the same restrictions on resistor value as IC designers, the Widlar circuit is still useful in a number of applications, such as supplying the tail current for a long-tailed pair differential amplifier, intended to operate at low currents, and for providing a constant current for the generation of extended duration linear sawtooth voltage sweeps. This is because it offers a number of attractive features, which include the following: low component count; large output voltage compliance; an output current relatively insensitive to supply rail voltage variations.

The circuit receives only a cursory textbook treatment, perhaps because of its apparent simplicity. Nevertheless, that superficial simplicity obscures some hidden subtleties. This article takes a closer look at the Widlar circuit, with the emphasis on design. That involves the subject of circuit tolerancing, an important practical topic, rarely taught and usually ignored in the literature.

Finally, there is a brief review of two system units that may be regarded as having their origins in the Widlar configuration. They are a temperature transducer, and a voltage reference source.

## Widlar basics

The Widlar current mirror is shown in Fig. 1, in which  $I_D$  is the drive, or input, current and  $I_0$  ( $\ll I_D$ ) is the output current.

The BJTs,  $Q_1$  and  $Q_2$  comprise a matched monolithic pair, fabricated close together on the same IC chip, such as is available with a BJT array. It must be emphasised that predictable circuit performance is not obtained using discrete BJTs for  $Q_1$  and  $Q_2$  for two reasons. First, there is no guarantee of close base-emitter voltage matching, an indispensable requirement for this configuration. Second, and related to the

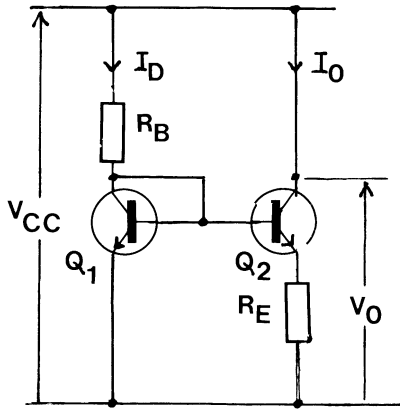


Fig. 1 The Widlar current mirror.

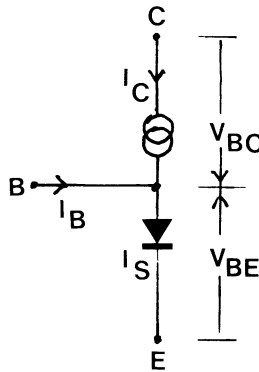


Fig. 2 Low current d.c. model of a BJT.

first, two discrete devices do not share the same intimate thermal environment as a monolithic pair. The BJT model of Fig. 2 is applicable for operation in the forward-active mode ( $V_{BC} < 0$ ) under low-level injection conditions but at terminal currents well above leakage levels.

The collector current  $I_C$  and the base current  $I_B$  are given by

$$I_C = I_S \exp(V_{BE}/T_T) \tag{1}$$

and

$$I_B = I_C/\beta \tag{2}$$

The current parameter  $I_S$  is dependent upon the properties of the base region. In particular, it is proportional to the base-emitter junction area and is typically of the order of  $10^{-15}$  A for a low power npn device.

The voltage parameter  $V_T$ , often referred to as the ‘thermal voltage’, is equal to  $86.2 \mu\text{V}/^\circ\text{C} \times T$ ,  $T$  being the absolute temperature ( $^\circ\text{C} + 273$ ):  $V_T \approx 25.8 \text{ mV}$  at a room temperature of 300 K.

The parameter  $\beta$  (typically, 100) is the common-emitter direct-current gain.

Experimental measurements<sup>2</sup> show that eqn (1) is valid over a range of many decades of  $I_C$  above  $V_{BE} = 4V_T (\approx 100 \text{ mV})$ , corresponding to  $I_C \approx 50I_S$ .

Above 1 mA, however, the model of Fig. 2 must be modified by the addition of a resistor in series with the base lead to allow for the potential drop in the base extrinsic resistance. An equivalent circuit for Fig. 1, using the model of Fig. 2 is shown in Fig. 3.

In a first-order analysis, we assume that  $Q_1, Q_2$  have identical characteristics and that base currents can be neglected. Then,  $I_{C1} = I_D, I_{C2} = I_0$  and

$$\Delta V = (V_{BE1} - V_{BE2}) \tag{3}$$

Hence, using eqn (1),

$$\Delta V = V_T \log_e(I_D/I_0) \tag{4}$$

Furthermore,

$$\Delta V = I_0 R_E \tag{5}$$

$$\text{Thus, } I_0 R_E = V_T \log_e(I_D/I_0) \tag{6}$$

If  $I_D$  is known and  $I_0$  is specified, the process of finding  $R_E$  is trivial, but that is about as far as a textbook treatment usually goes. Other problems in analysis are not so simple, as the following example shows.

In Fig. 4, the biasing circuit for the input stage of the classic 741 operational amplifier,  $I_0$  cannot be calculated directly from eqn (6) because the equation is transcendental (it has no closed form solution), so how to proceed systematically?

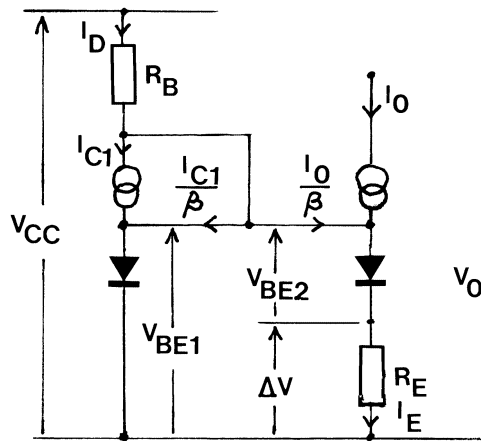


Fig. 3 D.c. equivalent circuit of Fig. 1.

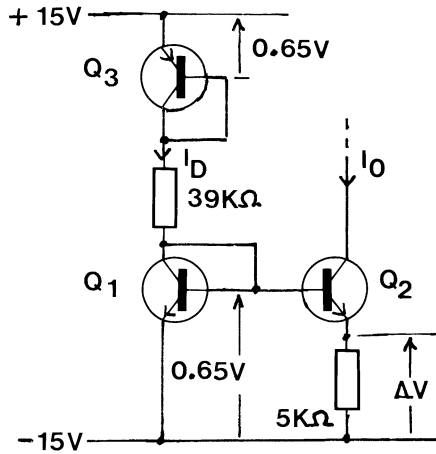


Fig. 4 Input-stage bias circuit of the 741 op amp.

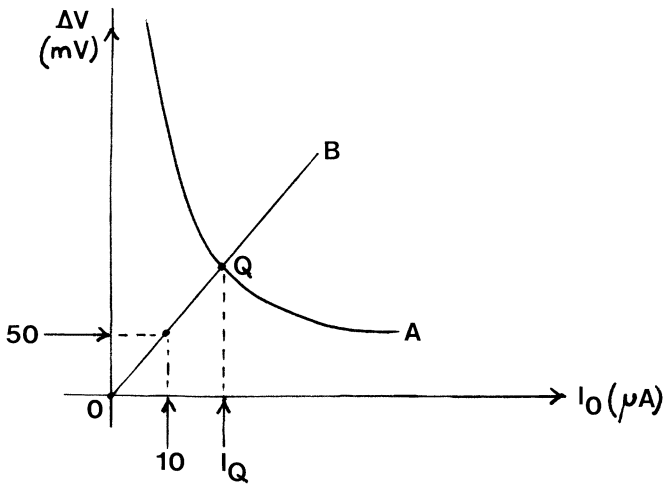


Fig. 5 Graphical determination of  $I_0$  in Fig. 4. A and B represent, respectively, eqns (4) and (5) in the text.

The graphical approach of Fig. 5 is helpful. Curve A represents eqn (4) for  $I_D = 0.74 \text{ mA}$ , based upon the assumption that  $V_{BE1} = V_{BE3} = 0.65 \text{ V}$ .

Line B is a graph of eqn (5): only two points are needed to draw this, convenient choices being the origin and a point X corresponding to  $I_0 = 10 \mu\text{A}$  and  $\Delta V = (10 \mu\text{A} \times 5 \text{ k}\Omega) = 50 \text{ mV}$ . The intersection point, Q, of A and B gives the operating current  $I_Q$ . A graph-paper plot gives  $I_Q \approx 19 \mu\text{A}$ .

An alternative, iterative, procedure for finding  $I_Q$  is indicated in Table 1. The step

TABLE 1 Iterative procedure for finding  $I_0$

Step	Assume	Calculate	→	From
1	$\Delta V = \Delta V_1$	$I_{01}$		$\Delta V_1/R_E$
2	$I_0 = I_{01}$	$\Delta V_2$		$V_T \log_e(I_D/I_{01})$
3	$\Delta V = \Delta V_2$	$I_{02}$		$\Delta V_2/R_E$
4	$I_0 = I_{02}$	$\Delta V_3$		$V_T \log_e(I_D/I_{02})$
5				

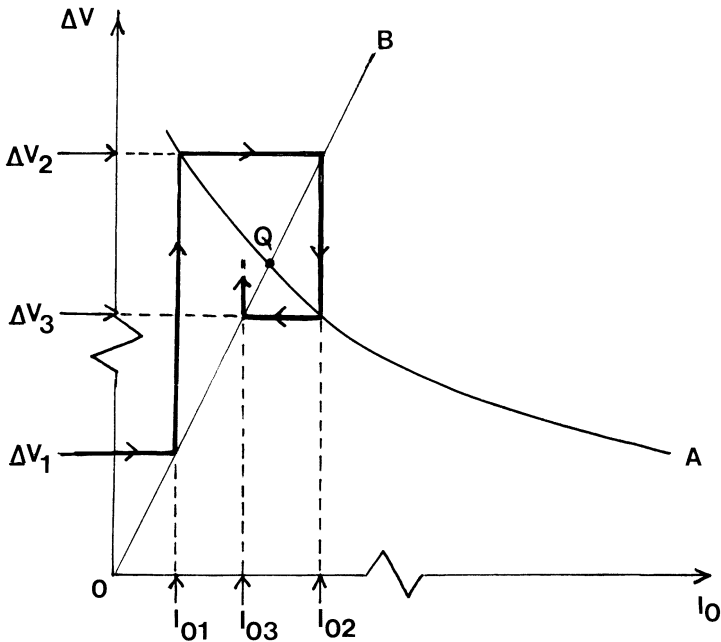


Fig. 6 Graphical background to iterative procedure.

sequence starts by assuming an arbitrary, but convenient, value of  $\Delta V$  (e.g.  $\Delta V_1 = 50\text{ mV}$ ) and ends when two successive values of  $I_0$  differ by less than a chosen percentage, for example less than 1%. The ‘cobweb’ diagram of Fig. 6 is a graphical justification for this numerical approach: the arrows show how sequential values of  $I_0$  converge to the final value  $I_Q$ . In practice, only a few steps are normally required to achieve a value of  $I_0$  sufficiently close to  $I_Q$ .

In contrast to analysis, the process of design involves selecting  $R_E$ ,  $R_B$  to obtain a specified  $I_Q$ . The problem then is that there is no unique choice for  $R_E$ ,  $R_B$ . As Fig. 7 makes clear, any pair of values such as  $R_{E1}$ ,  $R_{B1}$ , etc., is suitable. Consequently, it is necessary to develop criteria for their choice. That involves a closer look at the accuracy of eqn (6) and a study of circuit tolerances.

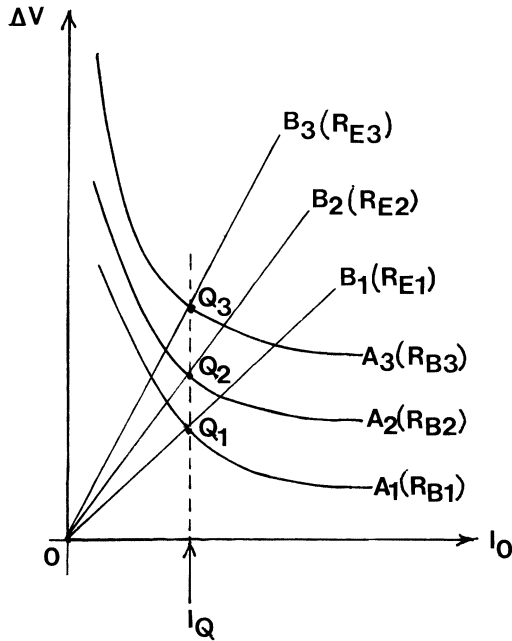


Fig. 7 For a specified  $I_0$  there is no unique choice for  $R_B, R_E$ .

**Base current effects**

Referring to Fig. 3, and summing currents at the collector of  $Q_1$ ,

$$I_{C1} = [I_D - (I_0/\beta)]/[1 + (1/\beta)] \tag{7}$$

As  $I_D \gg I_0$  and  $\beta \gg 1$ , the second term in the numerator of eqn (7) is negligible compared with the first. Therefore,

$$I_{C1} = \alpha I_D \tag{8}$$

where  $\alpha = \beta/(1 + \beta)$  is the common-base direct-current gain.

Hence, for  $Q_1$  eqn (1) gives

$$V_{BE1} = V_T \log_e(\alpha I_D/I_{S1}) \tag{9}$$

For  $Q_2$ ,

$$V_{BE2} = V_T \log_e(I_0/I_{S2}) \tag{10}$$

Using eqn (3),

$$\Delta V = V_T \log_e(\alpha I_D/I_0)(I_{S2}/I_{S1}) \tag{11}$$

With perfectly matched BJTs,  $I_{S1} = I_{S2}$  so in that nominal case, the following modified form of eqn (4) is applicable:

$$\Delta V = V_T \log_e(\alpha I_D/I_0) \tag{12}$$

A modified form of eqn (5) is obtained by replacing  $I_0$  by  $(I_0/\alpha)$ . Then,

$$\Delta V = I_0 R_E/\alpha \tag{13}$$

A more accurate version of eqn 6 is thus,

$$I_0 R_E/\alpha = V_T \log_e(\alpha I_D/I_0) \tag{14}$$

To find the nominal value of  $I_0$  we can use either a graphical procedure or the iterative approach, with the assumption that  $\alpha = 0.99$ .

**Tolerance effects**

Tolerancing the circuit involves quantifying the effect on  $I_0$  of supply voltage variations and manufacturing parameter spreads of all the components used.

Consider first the departure from unity of the ratio  $(I_{S2}/I_{S1})$ . Equation (11), written in a different form is

$$\Delta V = V_T \log_e(\alpha I_D/I_0) + V_T \log_e(I_{S2}/I_{S1}) \tag{15}$$

The second term on the right-hand side of the this equation is equal to the difference between  $V_{BE1}$  and  $V_{BE2}$  when  $Q_1$  and  $Q_2$  are both passing the same collector current. This is the base-emitter offset voltage of the pair. Only its magnitude,  $V_{OS}$ , is specified on manufacturers' data sheets for matched arrays and dual-matched BJTs so a plus and minus sign must be used with it in calculations.

Equation (15) now becomes

$$\Delta V = V_T \log_e(\alpha I_D/I_0) \pm V_{OS} \tag{16}$$

The effect of finite  $V_{OS}$  on  $I_0$  is best appreciated graphically. In Fig. 8, curve  $A_0$  represents eqn (12) and curve  $A_1$  represents eqn (16): it is eqn (12) shifted bodily up the  $\Delta V$  axis by an amount  $V_{OS}$ , here taken arbitrarily as positive and grossly exaggerated in magnitude for clarity. Line B represents eqn (13).

The existence of  $V_{OS}$  causes the operating point to move from  $Q_0$  to  $Q_1$ , corresponding to a small increase  $\delta I_0$  in  $I_0$ . This is associated with voltage changes  $R_E \delta I_0/\alpha$  across  $R_E$  and  $V_T \delta I_0/I_0$  in  $V_{BE2}$ . (The slope of  $A_0$  at  $Q_0$  is  $-V_T/I_0$ .) Hence,

$$V_{OS} = \delta I_0 [(R_E/\alpha) + (V_T/I_0)] \tag{17}$$

This can be rearranged to give

$$(\delta I_0/I_0) = (V_{OS}/V_T)/(1+m) \tag{18}$$

where the newly introduced parameter  $m$  is given by

$$m = \Delta V/V_T = R_E I_0/(\alpha V_T) \tag{19}$$

It will be seen later that  $m$  is a key parameter in the design process.

Equation (18) explains entry 'd' in Table 2, which summarises tolerance effects. The other entries (a, b, c, e) can be explained by a graphical argument or, more easily, calculated by applying the rules of partial differentiation to eqn (14).

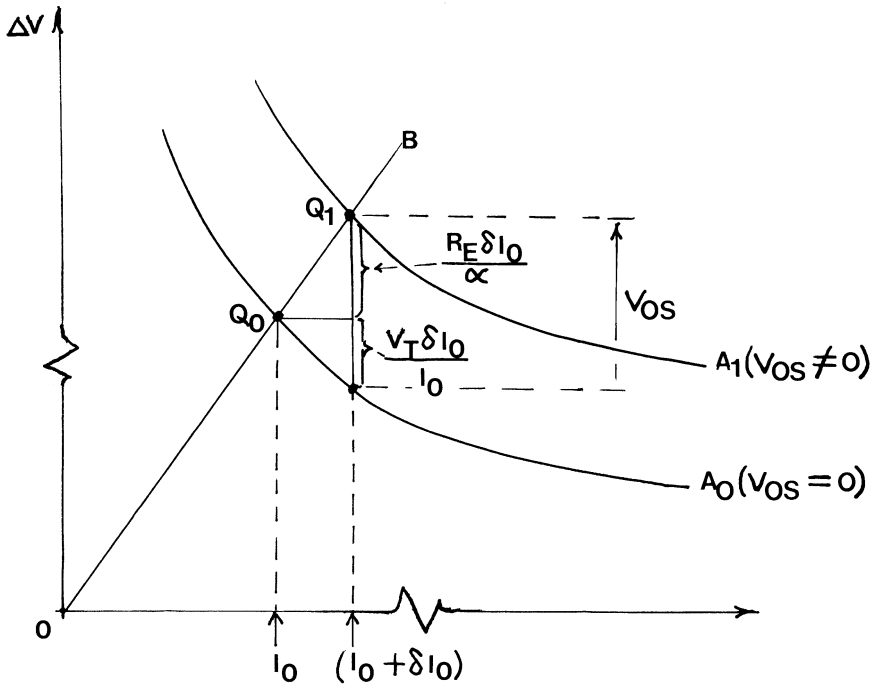


Fig. 8 Showing, quantitatively, how a finite offset voltage  $V_{OS}$  for  $Q_1, Q_2$  changes  $I_0$ .

TABLE 2 Showing the fractional tolerance contributions to  $I_0$

Source of tolerance	$ \delta I_0 / I_0 ^*$
$R_E$	$a = \{m/(1+m)\}(\delta R_E / R_E)$
$R_B$	$b = \{1/(1+m)\}(\delta R_B / R_B)$
$(V_{CC} - V_{BE1})$	$c = \{1/(1+m)\} \{ \delta(V_{CC} - V_{BE1}) / (V_{CC} - V_{BE1}) \}$
$V_{OS}$	$d = \{1/(1+m)\}(V_{OS} / V_T)$
$\alpha$	$e = \delta\alpha / \alpha$

\*  $m = \Delta V / \Delta V_T = I_0 R_E / (\alpha V_T)$

The desensitisation factor  $(1 + m)$  is reminiscent of the similar factor  $(1 + A\beta)$  in amplifier theory and arises for the same reason, the presence of negative feedback. The worst case tolerance WCT is given by

$$WCT = \pm(a + b + c + d + e) \tag{20}$$

A figure for the most probable tolerance (MPT) is obtained by taking the root sum of the squares, since the random variables are uncorrelated.

TABLE 3 Contributions to  $TCI_0$ , the temperature coefficient of  $I_0$

Temperature variable element	$TCI_0^\dagger$
$R_E$	$- \{m/(1+m)\}TCR_E$
$R_B$	$- \{1/(1+m)\}TCR_B$
$V_T$	$+ \{m/(1+m)\}(1/T)$
$\alpha$	$TC\alpha$

$^\dagger TCX = (1/X)(dX/dT)$

$$MPT = \pm(a^2 + b^2 + c^2 + d^2 + e^2)^{1/2} \tag{21}$$

**Temperature effects**

If  $I_D \leq 1$  mA, the power dissipation in  $Q_1$  and  $Q_2$  does not exceed 1 mW. The thermal resistance of top-hat metal packages containing two matched BJTs, and of 14-pin DIL plastic packages containing BJT arrays<sup>3</sup> is 0.16°C/mW. Hence, the junction temperature rise above ambient is negligible.

The contributions to the change in  $I_0$  due to ambient temperature change are summarised in Table 3. The temperature coefficient (tempco) of a variable  $X$  ( $R_E, R_B, \alpha$ ) is defined as  $TCX = (1/X)(dX/dT)$ , and is a signed quantity.

All the entries, except that for  $V_T$ , follow directly from Table 2. The variation of  $I_0$  with  $V_T$  also takes into account the offset voltage change and can be found by differentiating eqn (14). If  $R_E, R_B$  are of the same type,  $TCR_E = TCR_B = TCR$ , say. The TCRs of metal film, carbon composition and IC diffused resistors are respectively of the following order: 0.01%/°C; 0.15%/°C, and 0.2%/°C.  $TC\alpha \approx 0.01\%/°C$ .

In discrete component circuit designs using metal film resistors, and  $m = 4$ ,  $TCI_0 \approx 0.27\%/°C$  and is dominated by the variation of  $V_T$ . The variation of  $V_{BE1}$  contributes a negligible amount, when using 15 V supplies, since it changes by only some 2 mV/°C. For IC designs  $TCI_0 < 0.1\%/°C$ .

**Output resistance**

The incremental output resistance,  $R_0$ , at the collector of  $Q_2$  in Fig. 1 is given by<sup>4</sup>

$$R_0 = (V_A/I_0) \left[ 1 + \left\{ \beta \Delta V / (\Delta V + \beta V_T) \right\} \right] \tag{22}$$

In this equation  $V_A$  is the Early Voltage. For the normal practical condition  $\beta \gg m$ , this reduces to

$$R_0 \approx (V_A/I_0)(1+m) \tag{23}$$

A rearrangement of this gives the fractional change in  $I_0$  with  $V_0$  directly,

$$(1/I_0)(\delta I_0/\delta T) \approx 1/[V_A(1+m)] \tag{24}$$

TABLE 4 Dependence of tolerance (%) contribution to  $I_0$  on  $m$  for:  $V_T = 25.8\text{ mV}$ ;  $V_{CC} = 15\text{ V} \pm 0.25\text{ V}$ ;  $V_{BE1} = 0.65 \pm 0.05\text{ V}$ ,  $\alpha = 0.99 \pm 0.01$ ; and, two values of  $V_{OS}$ ,  $5\text{ mV}$  and  $2\text{ mV}$ . Non-integer entries are rounded up to two significant figures

$m$	Tolerance (%) on $I_0$				
	$(a + b)$	$c$	$d$	$e$	
1	1	1.04	9.7	3.8	1
2	1	0.69	6.5	2.6	1
3	1	0.52	4.8	1.9	1
4	1	0.42	3.9	1.6	1
5	1	0.35	3.2	1.3	1
			$V_{OS} = 5\text{ mV}$	$V_{OS} = 2\text{ mV}$	

### Design procedure

The assumed design aim is to obtain a specified  $I_0$  with the closest tolerance using low cost components. Close tolerance (1%) high stability resistors are relatively inexpensive compared with BJT pairs with guaranteed close matching. For the low cost array type CA3046, a specified typical value of  $V_{OS}$  is  $0.45\text{ mV}$ . However, the maximum value is quoted as being  $5\text{ mV}$  and it is this figure upon which a worst-case design must be based. (For the more expensive BJT pair, type LM394, the maximum  $V_{OS}$  is  $0.1\text{ mV}$ .)

Table 4, derived from Table 2, shows tolerance contributions for 1% resistors:  $V_{CC} = 15\text{ V} \pm 0.25\text{ V}$ ,  $V_{BE1} = (0.65 \pm 0.05)\text{ V}$ ,  $\alpha = 0.99 \pm 0.01$ , and two values of  $V_{OS(\text{max})}$ ,  $2\text{ mV}$  and  $5\text{ mV}$ .

The effect of  $V_{OS}$  is reduced as  $m$  is increased but an upper limit to this parameter is set by the condition that  $I_D < 1\text{ mA}$  for eqn (1) to be applicable.

A proposed procedure for discrete circuit design is therefore as follows:

- Choose a preferred value of  $R_E$  from the 5% range, but with a 1% tolerance, so that  $m (= I_0 R / \alpha V_T)$  has the maximum value that meets the condition,

$$\log_e(1000/I_0(\mu\text{A})) > m \quad (25)$$

For this and subsequent calculations, assume that

$$V_T = (86.2 \times T)\mu\text{V} \text{ and } \alpha = 0.99$$

- Calculate  $I_D$  for the chosen value of  $m$ , using a rearranged form of eqn (14),

$$I_D = (I_0/\alpha)\exp(m) \quad (26)$$

- Calculate  $R_B$  using

$$R_B = (V_{CC} - 0.65)/I_D \quad (27)$$

- If the nominal resistance of the resistor (or combination of resistors), chosen from the preferred range, differs from that specified by eqn (27), by an amount  $r$  ( $\ll R_B$ ), then the nominal value of  $I_0$  differs from the target value by  $100r/[R_B(1+m)]\%$ .
- Estimate the tolerance on  $I_0$ , using Table 4 with the appropriate value of  $V_{CC}$ . From the data in the table, the choice  $m = 4$  together with  $V_{OS} = 5\text{ mV}$ , gives  $\text{WCT} \approx \pm 6.3\%$  and  $\text{MPT} \approx \pm 4.2\%$ .
- Estimate  $\text{TC}I_0$  with the aid of Table 3.
- Determine the change in  $I_0$  with  $V_0$ , from its target value at  $V_0 = 0.7\text{ V}$ , using eqn (24). In the absence of a specified  $V_A$ , or other data from which it can be deduced, assume a default value of  $100\text{ V}$ . Thus, for  $m = 4$ ,  $I_0$  increases by  $0.2\%$  per volt increase in  $V_0$ .

A refinement to the procedure allows for the fall-off in  $\beta$  with decrease in collector current. For example, the specification (RCA) for the CA3046 lists  $\beta(\text{typ})$  as 100 at  $I_C = 1\text{ mA}$  falling to 50 at  $I_C = 10\text{ }\mu\text{A}$ . To cater for this, use  $\alpha = 0.98$  ( $\beta = 49$ ) in the calculation of  $m$  for eqn (25) and  $\alpha = 0.99$  ( $\beta = 99$ ) for the calculation of  $I_D$  using eqn (26).

Although the 741 was conceived over 30 years ago, criteria for resistor choice for the Widlar biasing scheme have not, so far as this author is aware, been published. Nevertheless, it is instructive to consider the designated IC values in the light of the design proposals made above for a discrete-component design.

Neglecting base currents, the requirement  $I_0 = 19\text{ }\mu\text{A}$  and the choice  $R_E = 5\text{ k}\Omega$  gives  $\Delta V = 95\text{ mV}$  and  $m = 3.68$ . Hence,  $I_D = 19 \exp(3.68)\text{ }\mu\text{A} = 753\text{ }\mu\text{A}$  and  $R_B = 38\text{ k}\Omega$ , compared with the  $39\text{ k}\Omega$  shown on circuit diagrams. This difference is not significant when it is remembered that integrated circuit diffused resistors do not normally have a tolerance closer than  $10\%$ .

If the design aim had been to produce  $I_0 = 19\text{ }\mu\text{A}$  using the minimum total circuit resistance, a possible requirement in IC technology, an unacceptable value of  $I_D$  would have resulted, as the following brief analysis shows.

Let

$$R_T = R_E + R_B \quad (28)$$

From eqn (19),  $R_E = (m\alpha V_T/I_0)$  and from eqns (26) and (27),

$$R_B = \alpha(V_{CC} - V_{BE1})/I_0 \exp(m)$$

Substituting these expressions for  $R_E$  and  $R_B$  in eqn (28), differentiating with respect to  $m$  and equating the result to zero gives

$$R_{T(\min)} = (\alpha V_T/I_0) \left[ 1 + \log_e \left\{ (V_{CC} - V_{BE1})/V_T \right\} \right] \quad (29)$$

Inserting numerical data,  $R_{T(\min)} = 10.77\text{ k}\Omega$ . Of this,  $R_B$  accounts for only  $1.33\text{ k}\Omega$ . This would result in the absurdly high figure of  $21.3\text{ mA}$  for  $I_D$ , at which current level eqn (1) would be inapplicable anyway.

To conclude this study of the Widlar circuit, two application examples are considered, briefly, in the following section.

### Related circuits

Versions of the Widlar configuration constitute the core of two important IC products, a temperature transducer<sup>5</sup> in which the output current is proportional to absolute temperature (PTAT), and a bandgap voltage reference.<sup>6</sup>

In a rudimentary form of the transducer (Fig. 9) the emitter areas of  $Q_1$ ,  $Q_2$  are scaled in the ratio  $1:n$  and those of  $Q_3$ ,  $Q_4$ , which comprise a pnp current mirror, are in the ratio  $1:p$ . The collector current of  $Q_4$ , which corresponds to  $I_D$  in the discussion of the basic Widlar mirror, is thus  $pI_0$ . Ignoring base currents,

$$\Delta V = I_0 R_E = V_T \log_e(pI_0/I_S) - V_T \log_e[I_0/(nI_S)] \quad (30)$$

Hence,

$$I_0 = (V_T/R_E) \log_e(pn)$$

and

$$I_T = (p+1)(V_T/R_E) \log_e(pn)$$

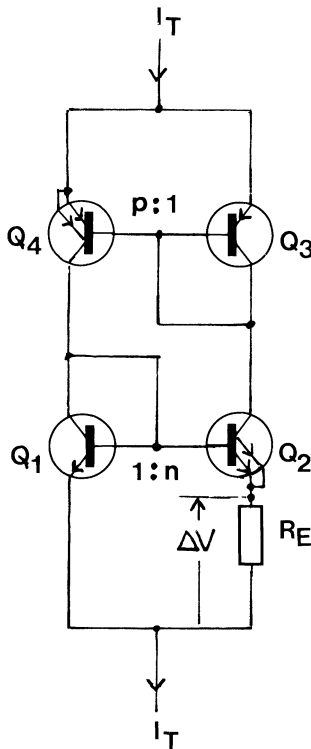


Fig. 9 Rudimentary temperature transducer:  $I_T \propto T$ .

But

$$V_T = (86.2 \times T)\mu V$$

so, if  $R_E$  is independent of  $T$ ,

$$I_T = CT \tag{31}$$

where the scale-factor  $C$  is given by

$$C = [(p+1)/R_E] \log_e(pn) \tag{32}$$

The design of refined versions of the circuit of Fig. 9 takes account of base currents and the Early Effect. By using a low tempco thin-film, laser-trimmed, resistor for  $R_E$  it can be arranged that  $C = 1 \mu A/K$ , as in the AD590 (Analog Devices).

The bandgap voltage reference is so-named because the output voltage is related to a fundamental property of silicon, the energy gap between the valence and conduction bands extrapolated to zero degrees absolute.

A basic form of the circuit is shown in Fig. 10. In this,  $Q_1, Q_2$  have an emitter area ratio  $1:n$  but are forced, by the action of amplifier  $A$ , to pass equal collector currents. Neglecting base currents,

$$\Delta V = I_0 R_E = V_T \log_e(n) \tag{33}$$

The output voltage  $V_R$  is thus given by

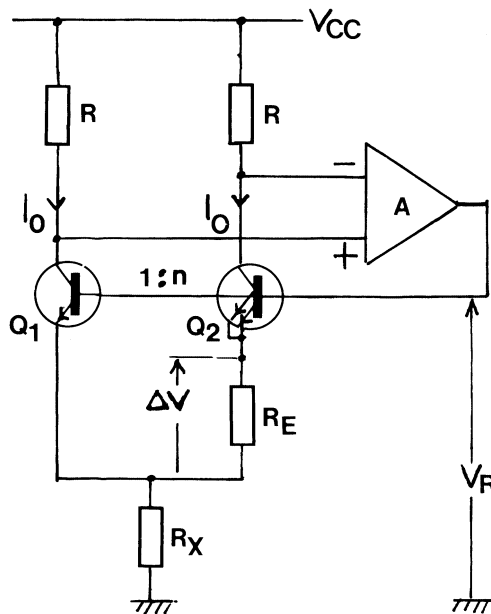


Fig. 10 Schematic circuit of voltage reference source.  $TCV_R$  is only a few  $ppm/^{\circ}C$  in practical designs.

$$V_R = V_{BE1} + 2V_T(R_X/R_E) \log_e(n) \quad (34)$$

The first item on the right-hand side of this equation decreases with  $T$  and the second one increases with  $T$ . If  $R_X$ ,  $R_E$ , and  $n$  are chosen so that  $V_R$  is near the bandgap voltage ( $V_{G0}$ ) for silicon, then  $TCV_R$  can be as low as a few parts per million, per degree kelvin.

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