The common-mode rejection ratio of a long-tailed pair

Bryan Hart
Leigh-on-Sea, Essex, UK

Abstract A graphical study, proposed here as an alternative to existing analytical methods, offers added circuit insight into the common-mode rejection ratio of a long-tailed pair differential amplifier using bipolar-junction transistors.

Keywords amplifier design; c.m.r.r

A study of the common-mode rejection ratio (c.m.r.r.) of a long-tailed pair (l.t.p.) provides a useful introduction to a parameter that is important in the design of a differential amplifier for use with low-level transducer outputs that may be contaminated by extraneous signals.

In such a study there are at least two well-established approaches. The first involves a straightforward application of Kirchhoff's Laws to a small-signal equivalent circuit of the stage. A shortcoming of this is that the manipulation of the algebra can easily distract attention from the details of circuit operation. The second approach involves an understanding of the concept of circuit bisection, which is applicable to certain classes of symmetrical configuration. This method is admirably concise but, arguably, better suited to those beginners with a feeling for the subtleties of circuit theory.

An alternative, graphical, approach introduced here is intended to offer added insight into circuit operation. A consideration of permissible input signal amplitudes, a topic normally neglected, features prominently in this approach.

Signal composition

Fig. 1 shows a basic l.t.p. configuration. Following normal practice in an introductory study, the respective parameters of the transistors Q_1, Q_2 are assumed to be identical. Their bases are initially held at the same potential, in this case earth. The base potentials are then raised by small voltage increments v_1 and v_2 respectively. Consequently the (commoned) emitter potential increases by v_e. We now express v_1, v_2, in terms of a 'common-mode' component, v_c, and a 'difference' (or, 'differential') mode component, v_d, which are defined as follows:

$$v_d = (v_1 - v_2) \tag{1}$$

and $$v_c = \frac{(v_1 + v_2)}{2} \tag{2}$$

It follows from eqns (1) and (2) that

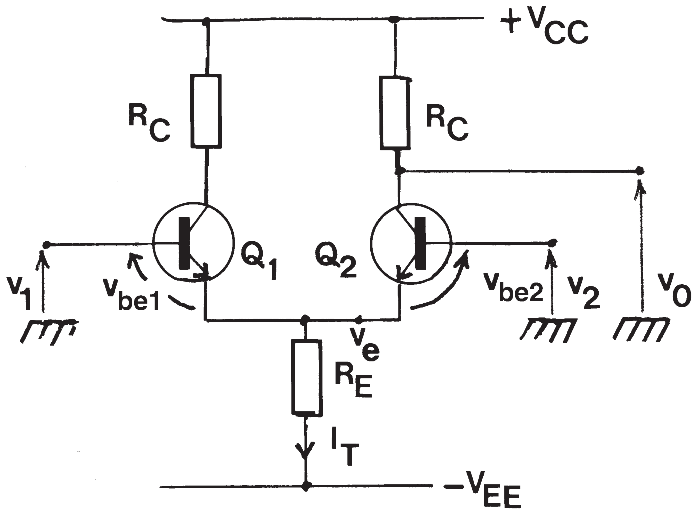

Fig. 1 *A basic long-tailed pair (l.t.p.) with input signals* v_1, v_2 *and output signal* v_o.

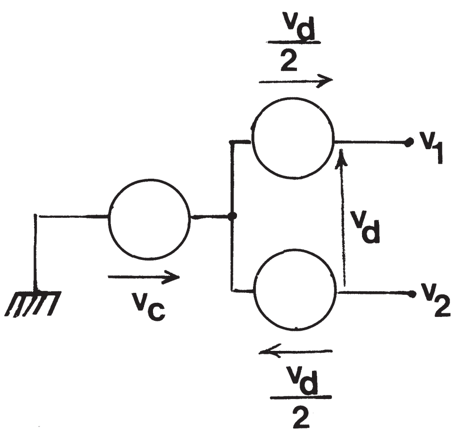

Fig. 2 v_d, v_c *are respectively the difference-mode and common-mode components of* v_1, v_2.

$$v_1 = v_c + \frac{v_d}{2} \tag{3}$$

and $$v_2 = v_c - \frac{v_d}{2}. \tag{4}$$

This resolution of v_1 and v_2 into v_d and v_c is depicted in Fig. 2. Suppose we arrange that $v_1 = -v_2 = v$: then, $v_c = 0$ and the double-ended input is subject solely to differential drive v_d (=2v).

The output voltage, v_{od}, resulting from this is

$$v_{od} = A_d v_d \tag{5}$$

where A_d is the small-signal differential voltage gain. If, instead, we operate with $v_1 = v_2 = v_c$, then $v_d = 0$ and the input drive is solely common-mode.

The output voltage, v_{oc}, is then,

$$v_{oc} = A_c v_c \tag{6}$$

Here, A_c is the small-signal common-mode gain.

For the general case, v_d and v_c are both present. Then we can combine the contributions due to v_d and v_c, each taken separately, provided the system is linear, a crucial assumption in subsequent analysis.

In that case,

$$v_o = v_{od} + v_{oc} = A_d v_d + A_c v_c \tag{7}$$

The ability of the system to amplify v_d at the expense of v_c is conveniently quantified by a parameter known as the common-mode rejection-ratio (c.m.r.r), ρ, which is normally defined as

$$\rho = \left|\frac{A_d}{A_c}\right|. \tag{8a}$$

Expressed in decibels, as is usually the case,

$$\rho_{dB} = 20 \log_{10}\left|\frac{A_d}{A_c}\right| \tag{8b}$$

Signal amplitudes

A restriction on signal amplitudes for eqn (7) to be valid is set by the nature of the transfer characteristic of the active devices used. With appropriately numbered second subscripts (used, where necessary, later) for Q_1 and Q_2, a suitable d.c. expression relating collector current I_C, and emitter current I_E, to base-emitter voltage V_{BE} is

$$I_C = \alpha I_E = I_S \exp\left(\frac{V_{BE}}{V_T}\right). \tag{9}$$

In this, α is the common-case direct-current gain; I_S ($\sim 10^{-15}$ A, for low power npn transistors) is a current parameter dependent upon base doping and geometry; V_T ('thermal voltage') = kT/q, k being Boltzmann's constant, T the absolute temperature (≈°C +273) and q the magnitude of the electronic charge. At room temperature $V_T \approx 25\,\text{mV}$, a figure used in the calculations below.

Equation 9 is valid[1] for $1\,\text{mA} > I_C > 50\,I_S$ (corresponding to $V_{BE} \approx 4V_T \approx 100\,\text{mV}$). In this range it is applicable also to changes in I_C and V_{BE} at the 'low' frequencies (e.g., up to about 1 kHz) assumed in the analysis which follows.

The changes i_c, i_e and v_{be} are related by

$$(I_C + i_c) = \alpha(I_E + i_e) = I_S \exp\left[\frac{(V_{BE} + v_{be})}{V_T}\right]. \tag{10}$$

From eqns (9) and (10),

$$\frac{i_c}{I_C} = \left[\left\{\exp\left(\frac{v_{be}}{V_T}\right)\right\} - 1\right]. \tag{11a}$$

Retaining only the first three terms in the exponential series on the assumption that (v_{be}/V_T) will be small gives,

$$\frac{i_c}{I_C} = \frac{v_{be}}{V_T}\left[1 + \left(\frac{v_{be}}{2V_T}\right)\right]. \tag{11b}$$

The second term in brackets can be ignored if $|(v_{be}/2V_T)| << 1$. In engineering calculations, the condition $(a/b) << 1$ is generally considered to be met if $a \leq (b/10)$. Applying that criterion here, the requirement for i_c to be linearly proportional to v_{be} is $|v_{be}| \leq 5\,\text{mV}$.

Equation (11b) then reduces to

$$i_c = \frac{I_C}{V_T} v_{be} = \frac{\alpha I_E}{V_T} v_{be}. \tag{12a}$$

If $v_{be} = 5\,\text{mV}$ then

$$i_{c(\max)} \approx \frac{I_C}{5}. \tag{12b}$$

The output voltage caused by i_c flowing in a collector load resistor, R_C, is thus linearly related to v_{be}. Equation (7) is, therefore, valid for those values of v_d and v_c for which $|v_{be}| \leq 5\,\text{mV}$. This magnitude restriction and the justification for it are not usually mentioned in textbook treatments.

Equation (12a) can be obtained, directly, by differentiating eqn (9) but that procedure does not yield a maximum permissible value for v_{be}.

Initial d.c. conditions

When $v_1 = v_2 = 0$ in Fig. 1, the bases of Q_1 and Q_2 are at earth potential and the two identical base-emitter junctions are in parallel.

Hence, $$(I_{C1} + I_{C2}) = 2I_S \exp\left(\frac{V_{BE}}{V_T}\right). \tag{13}$$

This equation describes line (i) in Fig. 3. A further equation for $(I_{C1} + I_{C2})$ is obtained by inspection of the circuit:

$$-V_{EE} + (I_{E1} + I_{E2})R_E + V_{BE} = 0. \tag{14a}$$

Substituting $(I_{C1} + I_{C2})/\alpha$ for $(I_{E1} + I_{E2})$, and rearranging, gives

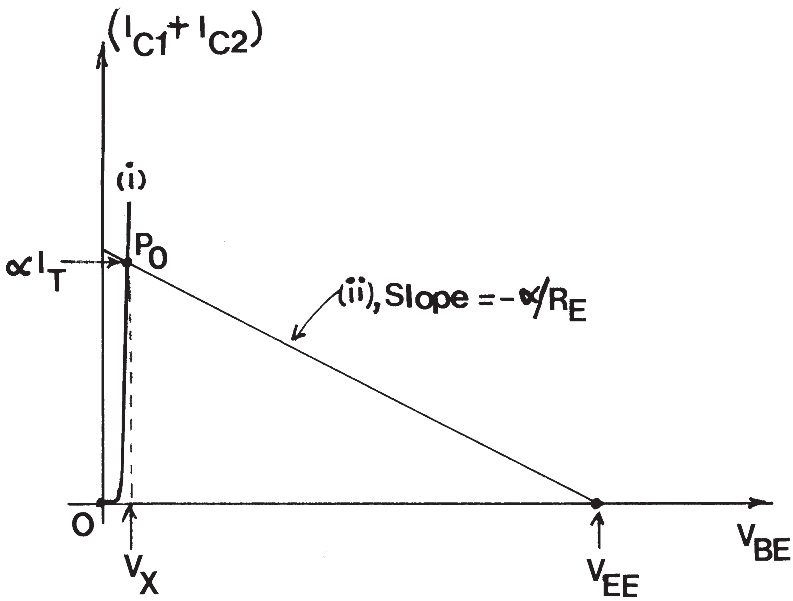

Fig. 3 *Graphical construction for initial d.c. conditions.*

$$(I_{C1}+I_{C2})=-\frac{\alpha V_{BE}}{R_E}+\frac{\alpha V_{EE}}{R_E}. \qquad (14b)$$

A plot of this gives the straight line, labelled (ii), in Fig. 3. It intersects line (i) at P_0 corresponding to the d.c. bias conditions $V_{BE} = V_X$ (i.e., emitter potential $-V_X$) and $I_{C1} = I_{C2} = \alpha I_T/2$.

Differential drive

For the input drive scheme of Fig. 4, $v_1 = -v_2 = v$ so $v_c = 0$ and $v_d = 2v$ ($\leq$10 mV). Because of the symmetrical nature of the circuit and the type of drive used, we make the plausible assumption, justified subsequently, that $v_e = 0$. Then Q_1 and Q_2 each effectively work in the grounded-emitter configuration for input signal variations and circuit operation is summarised in Figs 5 and 6.

As indicated in Fig. 5, the input signal v (= v_{be}) produces a current increase i_{cd} in the collector of Q_1. The signal $-v$ at the base of Q_2 causes an equal decrease in its collector current because it has already been established that the I_C/V_{BE} characteristic can be taken as linear in the vicinity of the bias point providing $|v_{be}| \leq 5$ mV. The net change in $(I_{C1} + I_{C2})$ is therefore zero, justifying the assumption that $v_e = 0$.

Substituting $I_{E1} = I_{E2} = (I_T/2)$ in eqn (12a) and using the relationships $v_d = 2v$, $v_o = i_{cd}R_C$ gives

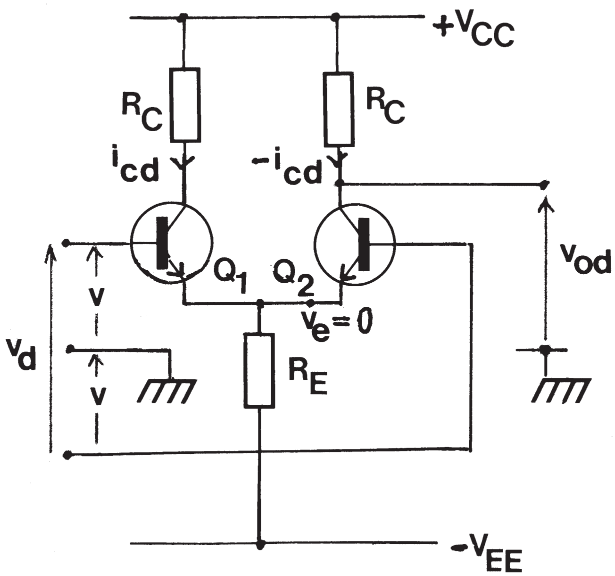

Fig. 4 *The l.t.p. driven solely by v_d.*

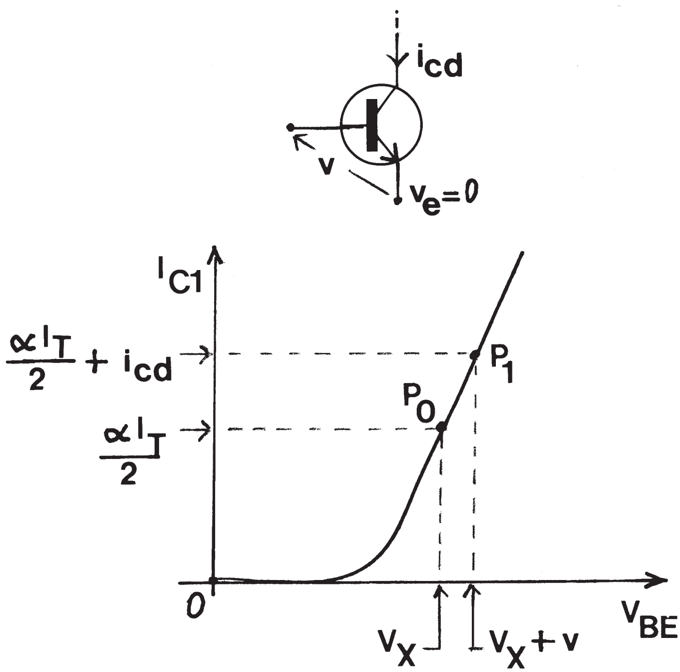

Fig. 5 *Operation of Q_1 in Fig. 4.*

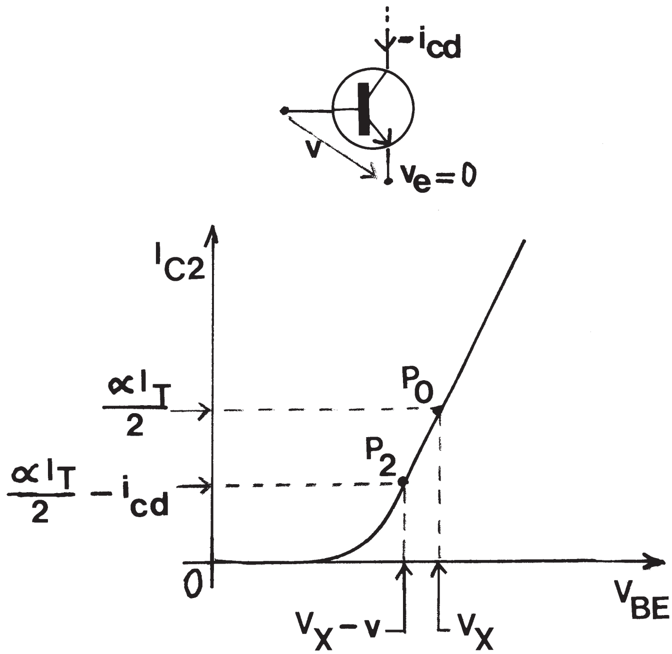

Fig. 6 *Operation of Q_2 in Fig. 4.*

$$A_d = \frac{v_{od}}{v_d} = \frac{\alpha I_T R_C}{4V_T}. \quad (15)$$

Thus, if $I_T = 1\,\text{mA}$ and $R_C = 10\,\text{k}\Omega$, then $A_D \approx 100$.

Common-mode drive

For the input drive scheme of Fig. 7, $v_1 = v_2 = v_c = v$ and $v_d = 0$. Circuit action is depicted in Fig. 8(a), which is a development of Fig. 3. When v is applied the operating point moves from P_0 to P_0', which is at the intersection of lines (i) and (iii). Line (iii) is, in effect, line (ii) shifted parallel to itself, along the V_{BE} axis, by an amount v. This is because v is added to the right-hand side of eqn (14a). Looking at this another way, the same change in I_T is produced if the bases of Q_1, Q_2 are fixed at earth potential and V_{EE} is changed to $-(V_{EE} + v)$. The total increase in collector current, $2i_{cc}$, is twice that in either transistor.

Fig. 8(b) shows a section of Fig. 8(a), enlarged for clarity, in the vicinity of P_0. For the assumed condition $|v_{be}| \leq 5\,\text{mV}$, $P_0\,P_0'$ is a straight line with slope $\alpha I_T / V_T$. From the geometry of the triangle $P_0\,P_0'\,S$, $v = v_{be} + v_e$ so,

$$v = \frac{2i_{cc}}{\alpha}\left[\frac{V_T}{I_T} + R_E\right]. \quad (16)$$

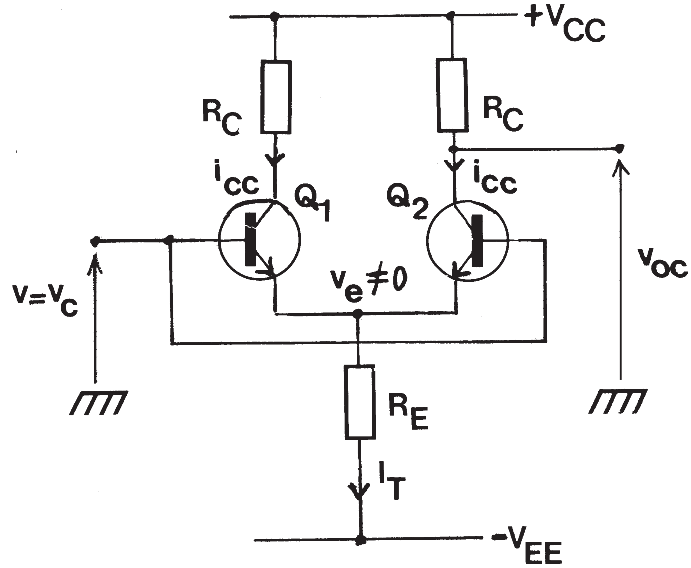

Fig. 7 *The l.t.p. driven solely by v_c.*

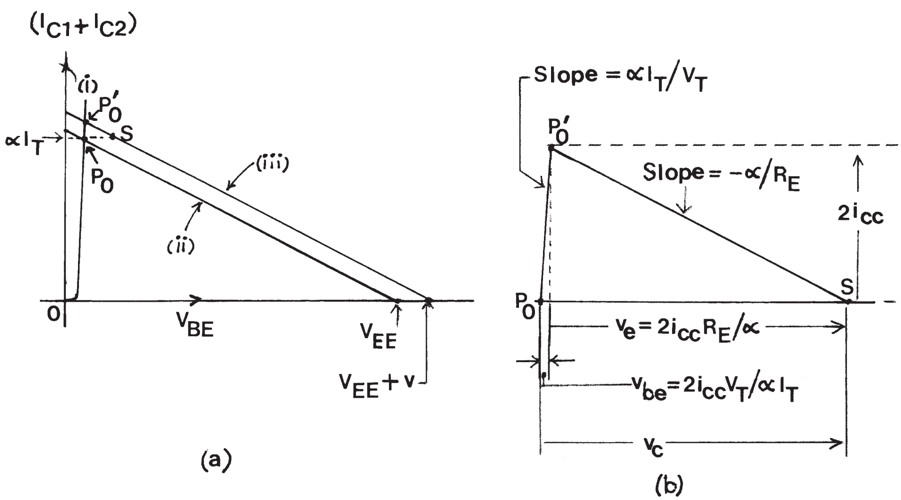

Fig. 8 *(a) Showing collector current change when v_c is applied; (b) enlarged section of (a) in the vicinity of* P_0.

Rearranging this and using the relationships $v_{oc} = -i_{cc} R_C$, $v = v_c$ gives

$$A_c = \frac{v_{oc}}{v_c} = -\frac{\alpha R_C I_T}{2[R_E I_T + V_T]}. \tag{17}$$

Normally, $R_C < R_E$, so $A_c < 0.5$.

Common-mode rejection ratio

Using the expressions for A_d, A_c, found above, in eqn (8a) and simplifying the result gives

$$\rho = \frac{(R_E I_T + V_T)}{2V_T}. \tag{18}$$

But $R_E\, I_T = (V_{EE} - V_X)$ and therefore

$$\rho = \frac{[V_{EE} - (V_X - V_T)]}{V_T}. \tag{19}$$

Normally, $V_{EE} \sim 15$ V, $(V_X - V_T) \sim 0.7$ V, so there is little error in writing, finally,

$$\rho = \frac{V_{EE}}{2V_T}. \tag{20}$$

This shows that for a given V_{EE}, ρ is independent of R_E, and, hence, of I_T (≤ 1 mA). From a circuit viewpoint this comes about because A_d and A_c are both directly proportional to I_T. The 10 mV magnitude restriction, mentioned earlier, applies to v_d but not to v_c. For $v_{be} = 5$ mV, the change in $(I_{C1} + I_{C2})$ is, from eqn (12b), approximately $I_T/5$ when v_c is applied. This means $v_{c(max)} \approx v_{e(max)} = (I_T R_E/5) = (V_{EE} - V_X)/5$. Typically, $v_{c(max)}$ exceeds $v_{d(max)}$ by well over two orders of magnitude, an attractive feature of the l.t.p.

For a given V_{EE}, a universally adopted method for increasing ρ above the value given in eqn (20) is to replace R_E by a current sink.

A tail current sink employing one or more bipolar junction transistors has an output characteristic of the form shown in Fig. 9: V_{EE} in eqn (20) is now replaced by the quantity $(V_{EE} + V_I)$, V_I being an 'intercept' parameter. Specific circuit configurations for three values of V_I in order of increasing magnitude are shown in Fig. 10, in which V_A represents[2] the 'Early Voltage' (typically, 100 V for a low power npn

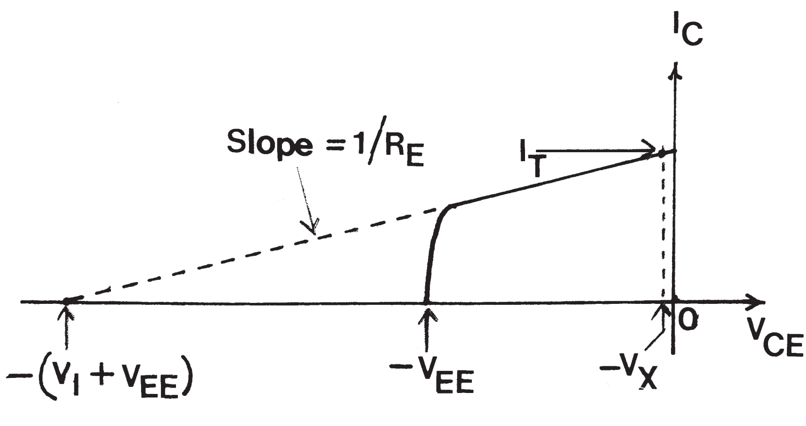

Fig. 9 *General form of current-tail characteristic (not to scale).*

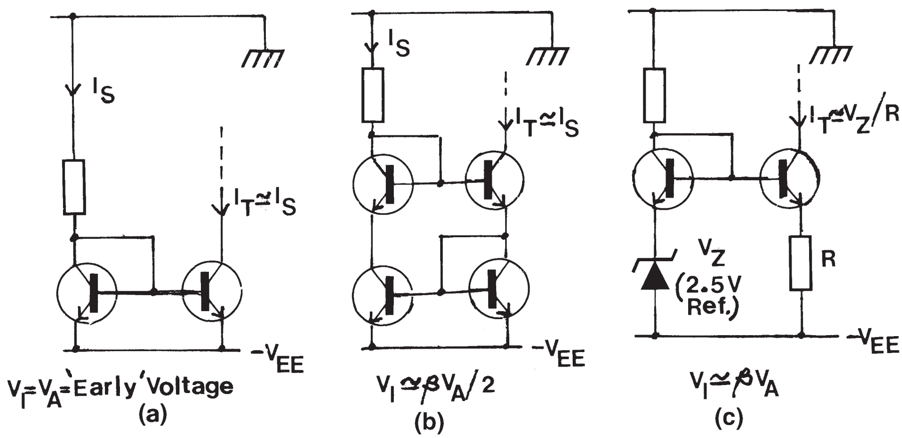

Fig. 10 *Three types of current tail with their values of* V_I. *(a) Simple current mirror; (b) modified Wilson current mirror; (c) common-base stage.*

device) and β is the common-emitter direct current gain (typically, ~100). The parameter ρ is increased by a factor F over that given by eqn (20): $F = [1 + (V_I/V_{EE})]$.

In conclusion, a note on the definition of ρ is appropriate. If, in Fig. 1, the 'output' is regarded as the difference between the collector potentials of Q_1 and Q_2, then ρ is theoretically infinite if these devices are perfectly matched. For practical devices, ρ is limited by their Early voltage matching[3]: ρ can be maximised by using cross-coupled transistor pairs, as in the well known 'biquad' scheme, and by using a bootstrapped-cascade configuration. These last two techniques are mentioned only in passing: further discussion of them goes beyond this introductory study.

References

1 R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits* (Wiley, Chichester, 1977), pp. 209–210.

2 B. L. Hart, 'Offset voltage, CMRR and PSRR of a long-tailed pair: an integrated approach', *Electron. Lett.*, **17** (15) (July 1981).

3 B. L. Hart, 'Early applied', *Electronics World*, July (1999), 591–594.